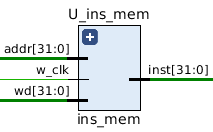
# Instruction Memory

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## 1.1 Implementation



IN PORT:

Addr[31:0]: 32 bits address

W\_clk: clock signal

Wd[31:0]: 32 bits of the value we want to write in the instruction memory.

OUT PORT:

Inst[31:0]: the result 32 bits instructions.

Each instruction has its own address, marked by the 32-bit vector of the program counter. When a given instruction is needed, the Instruction Memory delivers a 32-bit wide instruction. The following considerations have to be taken into account for the Instruction Memory:

• Each instruction is one word long (32 bits).

• Each instruction is addressed by a multiple of 4 bytes (1 word).

• Each instruction lies at a multiple of 4 bytes. By contrast, the program counter counts in terms of bytes. To avoid systematic “jumps” by four instructions when the new program counter is proposed, the program counter is divided by 4.

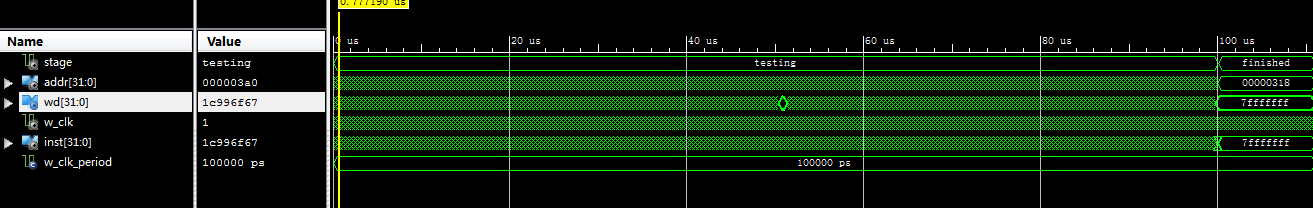
• At the rising edge of w\_clk, we write the value of the wd into instruction memory. In this way, it can support changing the program while our processor is running on the FPGA.

## 1.2 Testbench:

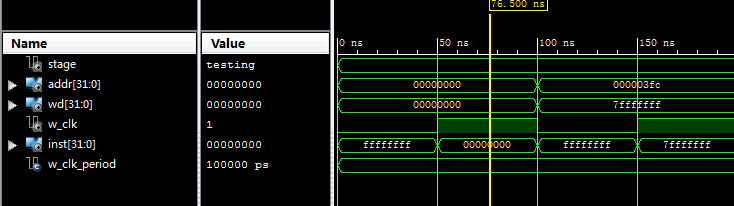
Random generate 1000 test cases.

1. Generate random variable to change addr(9 downto 2) and random variable to change instruction
2. When stage equals to finished, all the test case passed.

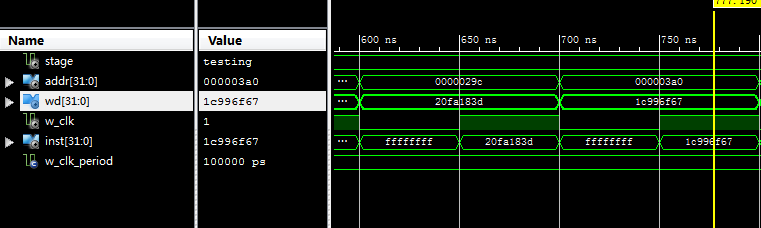
### 1.2.1 Function Simulation:



The stage is finished, which means all test cases passed.

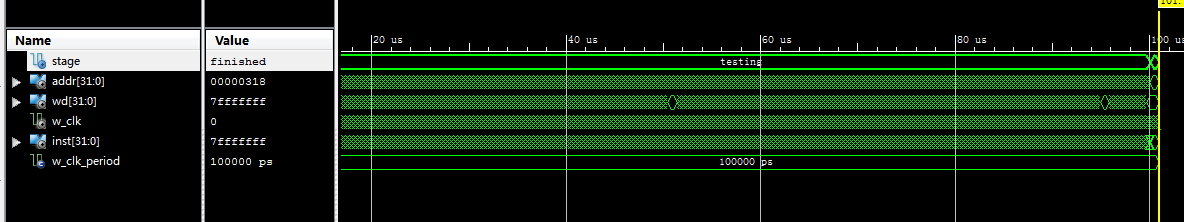


example1: the output instruction is the same as the wd value we wrote in.

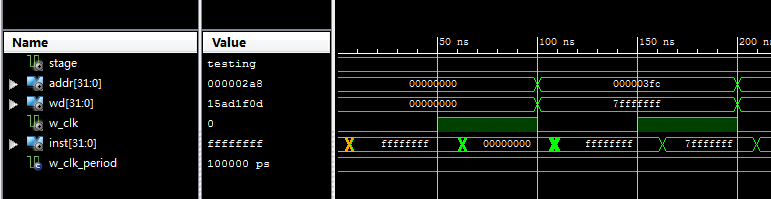


example2: the output instruction is the same as the wd value we wrote in.

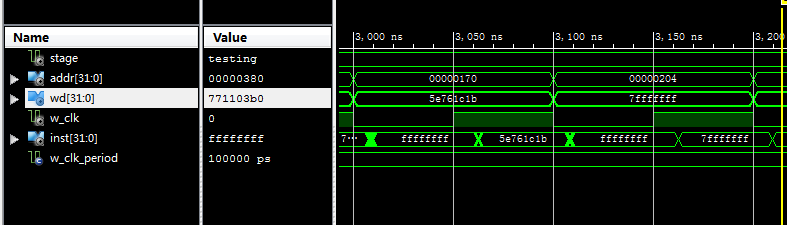
### 1.2.2 Timing Simulation:



The stage is finished, which means all test cases passed.



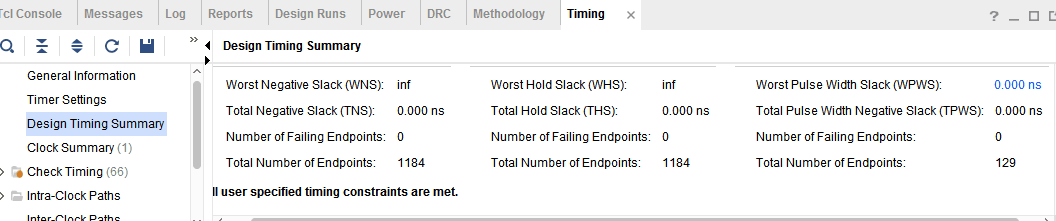
timing simulation for first example.



timing simulation for second example.

### 1.3 Analysis:

After several experiment, if we set the clock cycle as 1.82ns, we can get the timing summary as follows:





For the instruction memory part, the critical path delay is 1.82ns and the max frequency is 549.451MHZ. The latency is 1 clock cycle, so the propagation delay is 1.82ns.